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A TWO-TIER DEEMBEDDING TECHNIQUE FOR PACKAGED TRANSISTORS

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This paper describes a technique for deembedding transistor chip scattering parameters from the measurements of packaged devices in a standard transistor test fixture by the use of a set of secondary calibration standards, consisting of empty and specially wire-bonded transistor packages.

Introduction

Microwave transistor modeling and transistor circuit design require the accurate knowledge of the device two-port parameters. At microwave frequencies these are usually scattering parameters measured with a network analyzer. It is known that measurement errors due to analyzer imperfections can be greatly reduced by the use of accurately known calibration standards, and a number of error-correction procedures have been proposed[1-5]. The calibration standards, normally consist of an accurate 50-ohm termination (fixed or sliding), a good short circuit, an open circuit with a well known parasitic capacitance, and an accurate 50-ohm through line.

The most common method of measuring transistor scattering parameters at present is with packaged devices mounted on a microstrip test fixture. In some instances chip carriers are employed in place of packages to reduce the parasitic effects. The transistor is physically separated from the analyzer by the fixture and the package (or chip carrier) and their electrical properties obscure those of the transistor itself. The transistor scattering parameters must, therefore, be deembedded[6] by subtracting the effects of the fixture and the package from the measured scattering parameters.

The two tasks of analyzer error correction and device parameter deembedding are commonly done with the use of a single set of calibration standards. Because of the deembedding requirement, the connection of the calibration standards to the analyzer must be electrically identical to the connection of the device itself. This usually means that a special set of calibration standards must be developed, with the most difficult problem being the fabrication of an accurate broadband 50-ohm termination. The approach presented here attempts to by-pass some of these problems.

The Two-Tier Method

The two-tier method separates the analyzer error correction from the device deembedding. This allows the error correction to be done with reliable, manufacturer recommended coaxial APC-7 calibration standards and with available computer software. In this study, the twelve term error model[7] was used to correct for analyzer errors and to establish the measurement reference planes at the analyzer's APC-7 connectors.

The deembedding of the device scattering parameters ($s_{11}, s_{21}, s_{12}, s_{22}$) from the corrected measured values ($s_{11m}, s_{21m}, s_{12m}, s_{22m}$) was based on the signal flow diagram shown in Figure 1. In the figure, t represents the leakage path around the transistor chip, (u_{11}, u_T, u_{22}) represent the electrical connection between the transistor and port 1 of the analyzer, and (v_{11}, v_T, v_{22}) represent the connection to port 2. Because the embedding network is passive, the forward and reverse transmission terms are identical (u_T for the input and v_T for the output). There are seven embedding terms to be determined in order to be able to deembed the device parameters. Three calibration standards--an open circuit, input and output short circuits, and a through line--provide more than enough information, when measured, to determine the seven embedding terms. Once the embedding terms are known, the device parmeters can be obtained using the following equations:

$$s_{11} = [B\ (s_{11m} - u_{11})\ C\ v_{11}]/D$$
$$s_{22} = [A\ (s_{22m} - v_{22}) - C\ u_{22}]/D$$
$$s_{21} = u_T\ v_T\ (s_{21m} - t)/D$$
$$s_{12} = u_T\ v_T\ (s_{12m} - t)/D$$

where

$$A = u_T^2 + u_{22}\ (s_{11m} - u_{11})$$
$$B = v_T^2 + v_{11}\ (s_{22m} - v_{22})$$
$$C = (s_{21m} - t)\ (s_{12m} - t)$$
$$D = A\ B - C\ u_{22}\ v_{11}$$

The same equations were given by Rehnmark[8] in a different form.

Deembedding Experiment

The two-tier deembedding technique was tested on a 1-micron gate length GaAs MESFET packaged in a 70-mil ceramic stripline package. The device was fabricated on a VPE channel layer with a doping concentration of 8×10^{16} cm^{-3} grown on a semi-insulating buffer. A mesa etch was used for device isolation. TiPtAu was used for gate metal and was deposited in a 350 Å recess. AuGe/Ni source and drain ohmic contacts were 4 microns apart and the channel width was 300 microns. The device I_{dss} was 45 mA.

An empty transistor package served as the deembedding calibration standard for an open circuit. Because the package and all of its parasitic capacitances are a part of the embedding network, the empty package can be considered as an ideal open circuit and one needs to model only what is added inside the package. The short circuits were obtained by wire bonding from the input metallization to the ground metallization and from the output metallization to ground inside the package cavity of a second package. The through line was obtained by wire bonding between the input and the output metallizations of a third package. Multiple wire bonds were used to reduce the inductance.

The scattering parameter measurements were made with an HP8746B S-Parameter Test Set using an HP11608A Option 001 Transistor Fixture. The test fixture ground contact was milled to provide a 72-mil wide grounding bar for the package between the input and output 50-ohm microstrip lines. A 72-mil wide slot was cut in the grounding bar to accommodate the 70-mil package.

The electrical equivalents of the short-circuit and through-line wire bonds were obtained by a separate deembedding procedure, which consisted of the computer optimization of the equivalent circuits for the entire fixture, with and without packages, by fitting the measured scattering parameters from 2 to 12 GHz. This procedure evaluated the self-inductances of the input and output wire-bond shorts at 518 pH and 462 pH, respectively, with a 23 pH mutual component. The wire-bond through line had a characteristic impedance of 92 ohms and an electrical length of 10.75 picoseconds.

The reference planes for the deembedded device scattering parameters, because of our present choice of calibration standards, are located at the points of contact of the gate and the drain wire bonds with the input and the output package metallizations. In deriving the transistor equivalent circuit element values the wire bonds had to be taken into account.

Results

The embedding terms - t, u_{11}, u_T, u_{22}, v_{11}, v_T, v_{22} - were calculated from the measured scattering parameters of the fixture with each of the three calibration packages by an iterative procedure. The values of the transmission parameters (s_{21m}, s_{12m}) for the empty package and the package with the shorts were low and unreliable, and were not used in the calculation of the embedding terms. The resulting values of the embedding terms are given in Table I for frequencies 2 to 12 GHz. This is raw data, without any smoothing.

The scattering parameters were measured for the GaAs MESFET with a 3 volt bias on the drain and zero bias on the gate. Using the values of the embedding terms shown in Table I and the equations given above, the device scattering parameters were deembedded and the results are given in Table II. Again, this data was not subjected to any smoothing. The fluctuation of the resulting parameters is not much worse than the fluctuation of the original measured values. Only the low frequency values of s_{12}, where the amplitudes are low and subject to more measurement error, appear to be unreliable.

An equivalent circuit was optimized to fit the deembedded device scattering parameters. The equivalent circuit and the resulting element values are shown in Figure 2. The fit is quite good up to 10 GHz. Note that the gate and drain wire bonds are shown as transmission lines with given characteristic impedances and equivalent electrical lengths. This is an approximation, since the wire bonds loop and are not a constant distance from the ground plane.

Conclusion

It has been shown that the two-tier deembedding procedure can be used to obtain the equivalent electrical circuits for packaged (or chip-carrier mounted) transistors. It avoids the need for knowing the equivalent circuit of the package and for fabricating accurate 50-ohm terminations.

The accuracy of this procedure, however, can be enhanced in several ways. The use of packages with very low input-to-output capacitance would help to resolve the low values of device feedback capacitance more reliably. Since more than one package is involved, tighter package tolerances would reduce the deembedding errors. Lower inductance shorts and better through lines could be fabricated. The use of on-chip shorts and through lines could entirely eliminate the need for characterizing their equivalent circuits and would make the transistor wire bonds a part of the embedding network.

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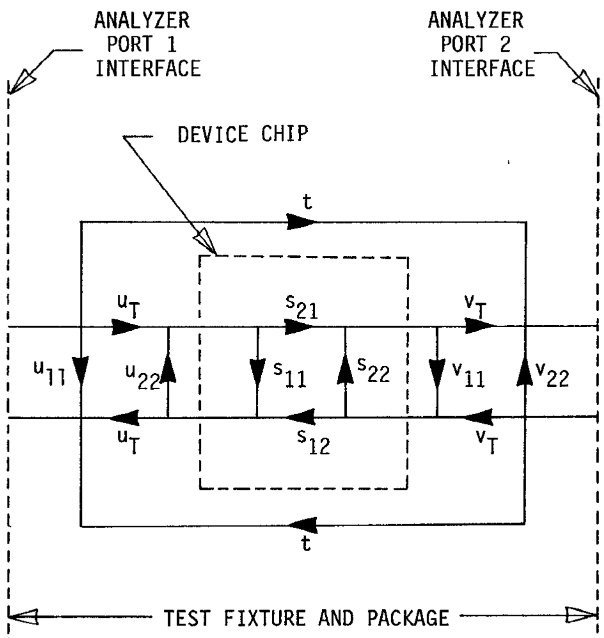


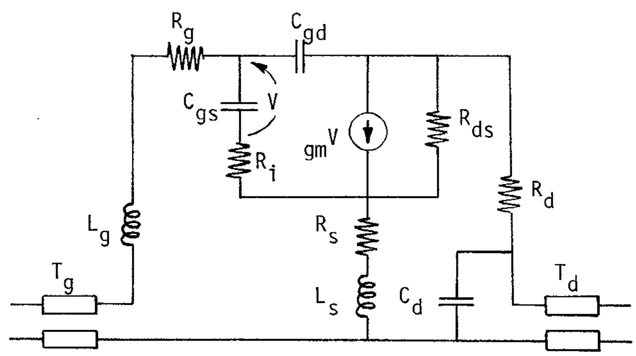
Figure 1. Equivalent scattering parameter representation of the fixture, the package, and the device chip.

Table I. Values of the embedding terms from 2 to 12 GHz.

f	t		u_{11}		u_t		u_{22}		v_{11}		v_t		v_{22}	
GHz	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG
2.	.099	94	.028	-56	.988	7	.003	179	.007	93	.984	7	.014	-43
3.	.112	95	.102	-65	.982	11	.011	-140	.011	50	.981	10	.071	-76
4.	.082	103	.170	-68	.982	15	.029	-107	.003	-163	.984	14	.128	-69
5.	.038	111	.198	-62	.980	20	.031	-107	.007	18	.979	18	.146	-69
6.	.007	-154	.201	-59	.983	25	.028	-130	.027	40	.973	22	.157	-73
7.	.056	-92	.204	-51	.974	30	.033	-114	.033	24	.975	26	.193	-68
8.	.106	-95	.299	-49	.977	33	.062	-75	.062	-15	.977	30	.279	-62
9.	.143	-124	.396	-51	.956	36	.146	-54	.144	-35	.961	33	.345	-64
10.	.155	-112	.457	-47	.930	39	.176	-55	.140	-34	.956	35	.359	-64
11.	.200	-113	.494	-45	.917	41	.195	-58	.155	-31	.948	37	.395	-67
12.	.272	-112	.487	-44	.927	44	.191	-56	.154	-33	.943	38	.355	-66

Table II. Deembedded scattering parameters of a 1-micron gate GaAs MESFET in a 70-mil ceramic stripline package.

f	s_{11}		s_{21}		s_{12}		s_{22}	
GHz	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG
2.	.934	-29	1.682	155	.047	-92	.797	-16
3.	.809	-44	1.605	136	.045	-88	.746	-21
4.	.681	-57	1.442	120	.031	-27	.697	-26
5.	.548	-73	1.406	101	.061	25	.656	-31
6.	.433	-97	1.376	83	.097	34	.630	-37
7.	.366	-127	1.406	65	.159	32	.570	-46
8.	.309	-172	1.316	46	.212	23	.465	-55
9.	.307	158	1.165	32	.248	2	.439	-57
10.	.334	137	1.173	27	.269	5	.4[illegible]	-57
11.	.350	119	1.187	18	.315	1	.46[illegible]	-53
12.	.417	102	1.159	4	.402	-4	.451	-61



$$g_m = g_{mo} \; e^{-j\omega\tau}$$

g_{mo}	= 21.8 mmhos	C_{gs}	= .209 pF
τ	= 3.70 pS	C_{gd}	= .073 pF
R_g	= 4.54 ohms	C_d	= .003 pF
R_i	= 38.3 ohms	L_g	= 196 pH
R_d	= 17.6 ohms	L_s	= 20 pH
R_{ds}	= 375 ohms		
T_g	= 176 ohms, 5.13 pS	transmission lines	
T_d	= 60.3 ohms, 2.33 pS		

Figure 2. Equivalent circuit of a 1-micron gate GaAs MESFET obtained from deembedded scattering parameters.